REMARKS

Remaining Claims

Nineteen (19) claims (Claims 1 and 4 - 21) are pending in the application. Claims 1, 4 – 10, 15, and 21 have been amended by the amendment being filed herewith. The Applicants respectfully request that the amendment be entered. Claims 6 and 15 are rejected under 35 USC §112, second paragraph. Claims 1, 10 and 21 are rejected under 35 USC §102(b). Claims 1, 4, 5, 7, 8, 10 – 13 and 16 - 18 are rejected under 35 USC §103(a). The Applicants respectfully traverse the rejections and request reconsideration.

Rejection of Claims 6 and 15 under 35 USC §112, second paragraph

Claims 6 and 15 stand rejected under 35 USC §112, second paragraph, as failing to particularly point out and distinctly claim that which the Applicants regard as the invention. Specifically, the Examiner states the term "bipolar junction transistor (BJT)" in claims 6 and 15 lacks antecedent basis.

Claim 6 refers to "at least one bipolar junction transistor (BJT)". The Applicants respectfully submit that the phrase "at least one" indicates that "bipolar junction transistor" is being introduced for the first time in the claims. Therefore, the Applicants do not believe that the phrase "bipolar junction transistor (BJT)" lacks antecedent basis. Nevertheless, claim 6 has been amended to ensure that no antecedent basis problems exist. Specifically, claim 6 has been amended to recite "at least a first bipolar junction transistor".

Prior to the amendment being filed with this response, claim 15 recited "using bipolar junction transistor process technology". Claim 15 has been amended by the amendment being filed herewith to recite "using a bipolar junction transistor process technology". The Applicants respectfully submit that this amendment removes any potential antecedent basis problems. Accordingly, the Applicants respectfully request that this rejection be withdrawn.

Rejection of Claims 1 and 10 under 35 USC §102(b) – Prior Art

Claims 1, 10 and 21 are rejected under 35 USC §102(b) as being anticipated by Applicants' admitted Prior Art. The Examiner reiterated the rejection set forth in the Office action of September 24, 2003, with the exception that the rejection is also applied against claim 21, which was added in the last response. The Applicants respectfully traverse the rejection and request reconsideration.

In the Examiner's response to the remarks made by the Applicants in the response filed on October 29, 2003, the Examiner agreed with the Applicants' statement that the prior art does not teach the protection diode being located inside of an IC comprising a buffer used to reduce delay on relatively long conductive signal lines. The Examiner stated:

"[t]hat statement is correct, but rejection [sic] is based on reason [sic] that claim language does not specifically require *the protection diode to be located inside an integrated circuit (IC) comprising a buffer used to reduce delay on relatively long conductive signal lines.* The claim language is only requiring 'a protection diode connected to the input of the first inverter'."

Although the Applicants believe that the preambles of the independent claims, prior to this amendment, do indicate that the protection diode is part of the IC, the claims have been further amended to clarify this point. Specifically, independent claims 1, 10 and 21 have been amended as follows:

1. An ~~buffer of an~~ integrated circuit (IC) having ~~the~~a buffer located therein for reducing delays on relatively long conductive signal lines of the IC, the buffer comprising:

a first inverter having an input connected to one of said conductive signal lines of the~~an~~ IC ~~that comprises the buffer~~;

a second inverter having an input connected to an output of the first inverter of the IC; and

a protection diode connected to the input of the first inverter, the protection diode pulling at least some electrical charge off at least one gate of at least one transistor of the first inverter to prevent the buffer from being damaged by too much electrical charge collecting on the transistor gate.

10. A method for preventing buffers used to reduce delays on relatively long conductive signal lines of an IC from being damaged due to electrical charges that collect on the buffers during manufacturing of the IC, the method comprising the steps of:

buffering at least one conductive signal line of an IC with a buffer to reduce delays in the conductive signal line, said buffer comprising first and second inverters, the first and second inverters, the buffer including a protection diode connected to an input of the first inverter, the protection diode pulling at least some of the electrical charge off of at least one gate of at least one transistor of the first inverter to prevent the buffer from being damaged by too much electrical charge collecting on said transistor gate, the buffer and the protection diode being contained in the IC.

21. A method for use in designing an integrated circuit (IC) comprising:

inserting buffer cells into an IC design such that respective inputs of the respective buffer cells are connected to conductive signal lines of the IC design for reducing delays on the conductive signal lines, each buffer cell including:

first and second inverters, the first and second inverters each having at least a non-inverting transistor and an inverting transistor with gates electrically coupled together, an output of the first inverter being connected to an input of the second inverter; and

a protection diode connected to an input of the first inverter inside of the IC.

The language of these claims clearly indicates that the IC comprises the buffer for reducing delays on relatively long conductive signal lines and that the buffer comprises the protection diode. Therefore, the Applicants believe that all of the independent claims in the present application clearly indicate that the protection diode is located inside of the integrated circuit. In other words, because the IC comprises the buffer and the buffer comprises the

protection diode, the protection diode is necessarily located inside of the integrated circuit.

Accordingly, the Applicants believe that this rejection is overcome and respectfully request that it be withdrawn.

Rejection of Claims 1, 5, 10 – 12 and 16 under 35 USC §103(a) – Kleveland et al. in view of Sigal

Claims 1, 5, 10 – 12 and 16 are rejected under 35 USC §103(a) as being unpatentable over Kleveland et al. (5,969,929) in view of Sigal (5,910,730). In view of the Examiner's comments indicating that the prior art does not teach a protection diode included in the buffer itself and inside of an integrated circuit, the Applicants believe, for the reasons stated above, that the clarification to the claims provided by this amendment overcomes this rejection. Accordingly, the Applicants respectfully request that this rejection be withdrawn.

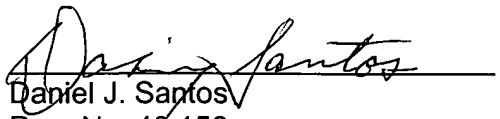
Rejection of Claims 4, 7, 8, 13, 17, and 18 under 35 USC §103(a) – Kleveland et al. in view of Sigal, and further in view of Shiota

Claims 4, 7, 8, 13, 17, and 18 are rejected under 35 USC §103(a) as being unpatentable over Kleveland et al. (5,969,929) in view of Sigal (5,910,730), and further in view of Shiota (5,426,322). For the reasons stated above, the Applicants believe that the clarification made to the claims by the amendment being filed herewith also overcomes this rejection. Accordingly, the Applicants respectfully request that this rejection be withdrawn.

CONCLUSION

For the reasons set forth above, it is respectfully submitted that all pending claims are now in condition for allowance, and Applicants request that a Notice of Allowance be issued in this case. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
GARDNER GROFF, P.C.



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